REMARKS

Claims 1-5, 7-10, and 12-15 are pending in this application, with claim 1 being independent. Claims 7-10 and 12 have been amended. Claims 6 and 11 have been previously canceled. Care has been taken to avoid introduction of new matter. Favorable reconsideration of the application in light of the following comments is respectfully solicited.

Claim Objections

Claims 7-10 and 12 were objected to under 37 C.F.R. 1.75(c) as being of improper form. Claims 7-10 and 12 have been amended to overcome this objection.

Claim Rejections – 35 U.S.C. § 102

Claims 1, 2, 5, 7-10, and 12 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent Number 6,003,051 ("Okazaki"). Applicants respectfully traverse this rejection for at least the following reasons.

Claim 1 recites a reproduction signal processing device including an A/D converter for quantizing an input analog reproduction signal into digital reproduction signal data; an adaptive equalizer for equalizing the reproduction signal data with a characteristic controlled according to data input to the adaptive equalizer and data output from the adaptive equalizer; and a PLL circuit for outputting a clock signal which is in synchronization with the reproduction signal data. The reproduction signal processing device also includes an analog filter for removing noise from the reproduction signal; a digital filter provided between the A/D converter and the adaptive equalizer, the digital filter equalizing the reproduction signal data with a fixed characteristic; and a control section for determining the fixed characteristic of the digital filter

during a learning period and setting, after the learning period, the characteristic of the digital filter by synthesizing the characteristic of the digital filter with a characteristic of the adaptive equalizer converged by the operation of the adaptive equalizer.

To provide context, in one implementation, the instant application is characterized in that a digital filter, which equalizes the reproduction signal data with a fixed characteristic, is provided between the A/D converter and the adaptive equalizer. And, the PLL circuit outputs the clock signal based on an output of the digital filter. With this configuration, reproduction signal data which has undergone the sampling and pre-equalization at an appropriate timing by the digital filter (e.g., digital filter 107 illustrated by FIG. 1) is input to the adaptive equalizing filter (e.g., adaptive equalizing filter 109 illustrated by FIG. 1). Application at page 18, lines 9-20. Therefore, PR equalization by the adaptive equalizing filter (109) is appropriately performed, and reproduction of recorded data by Viterbi decoder (e.g., Viterbi decoder 110 illustrated by FIG. 1) is performed. *Id.* Besides, the tap coefficients are fixedly set in the digital filter and therefore, pre-equalization and the PLL operation are performed without brining the feedback loop into unstable states, and reproduction of recorded data is performed with high accuracy. *Id.*

With this in mind, Applicants respectfully request reconsideration and withdrawal of the rejection of claim 1 and its dependent claims because Okazaki, at a minimum, fails to describe or suggest a reproduction signal processing device that includes, among other features, ***a digital filter*** provided between the A/D converter and the adaptive equalizer, the digital filter equalizing the reproduction signal data with a fixed characteristic, as recited in claim 1.

Okazaki, in FIG. 5, discloses a magnetic storing device that includes, among other features, a disk (1), a head (2), a head amplifier (6), an AGC amplifier (8), an analog filter (9), an

A/D converter (10), an FIR filter (11), and a maximum likelihood decoder (16). Okazaki at col. 7, line 35 to col. 8, line 23. In operation, head (2) reads a signal from disk (1) and provides the signal to head amplifier (6), which amplifies the signal and supplies it to AGC amplifier (8). Okazaki at col. 9, lines 30-36. The AGC amplifier (8) amplifies the signal to specific amplitude so that the signal may lie in the dynamic range of A/D converter (10). *Id.* The A/D converter (10) converts the signal into digital data, which is subjected to PR equalization at FIR filter (11). Okazaki at col. 9, lines 36-40. The output of the FIR filter (11) is connected to maximum likelihood decoder (16), which is for example Viterbi decoder and senses, according to a Viterbi algorithm, the most likelihood data string from PR-equalized digital data. *See e.g.*, Okazaki at col. 8, lines 44-51.

Turning to the pending Office Action with this overview in mind, the Office Action alleges that FIR filter (11) corresponds to the digital filter recited in claim 1 and maximum likelihood decoder (16) corresponds to the adaptive equalize also recited in claim 1. *See e.g.*, Office Action at page 3, lines 7-17. Applicants disagree because maximum likelihood decoder (16) is described to be a Viterbi decoder and not an adaptive equalizer. Okazaki at col. 8, lines 43-54. To this end, the alleged maximum likelihood decoder (16) appears to be similar to Viterbi decoder (110) illustrated by FIG. 1 of the instant application and not to adaptive equalizing filter (109) also illustrated by FIG. 1 of the instant application.

To illustrate further, in column 8, lines 44-54, Okazaki describes that maximum likelihood decoder (16) is configured to sense the most likelihood data string from PR-equalized digital data received from the FIR filter (11) and to output the sensed data to the decoder (17). *See e.g.,*, Okazaki at col. 8, lines 44-54 and lines 17-24 (stating maximum likelihood decoder (16) is, for example, a Viterbi decoder and senses the most likelihood data string from digital

data PR equalized according to a Viterbi algorithm and outputs the sensed data to decoder (17)). As such, it does not appear that maximum likelihood decoder (16) acts as an equalizer. That is, to the extent digital data are equalized, they appear to be equalized by FIR filter (11) and not by maximum likelihood decoder (16). *See e.g.*, Okazaki at col. 8, lines 17-22.

For at least these reasons, maximum likelihood decoder (16) does not correspond to the adaptive equalizer recited in claim 1. Moving forward, the instant application describes that the PR equalization is carried out by adaptive equalizer (109). *See e.g.*, Application at page 18, lines 12-14 and page 13, line 14 to page 14, line 10 (stating that in the adaptive equalizer (109) the tap coefficients are automatically updated to optimum values such that the equalization error is decreased, and thus, predetermined PR equalization suitable to the characteristics of the Viterbi detector (110) is performed). Therefore, it appears that FIR filter (11), which also performs PR equalization, *may* correspond to the adaptive equalizer filter recited in claim 1.[1]

Even assuming for the sake of argument that FIR filter (11) indeed corresponds to the adaptive equalizer recited in claim 1, Okazaki still fails to describe or suggest the digital filter recited in claim 1. Additionally, because Okazaki fails to describe or suggest the recited digital filter, it does not describe or suggest a control section for determining the fixed characteristic of ***the digital filter*** during a learning period and setting, after the learning period, the characteristic of ***the digital filter*** by synthesizing the characteristic of ***the digital filter*** with a characteristic of the adaptive equalizer converged by the operation of the adaptive equalizer, as recited in claim 1.

[1] Applicants previously submitted that Okazaki fails to describe or suggest the adaptive equalizer recited in claim 1. However, after carefully reviewing Okazaki in light of the newly issued Office Action, Applicants submit that Okazaki actually *may* describe the recited adaptive equalizer. Therefore and assuming, *arguendo*, Okazaki indeed describes the recited adaptive equalizer, Applicants apologize for any such misunderstanding and miscommunication and wish to clarify the record to indicate the same. However, as explained in the response, even assuming Okazaki discloses the adaptive equalizer, Okazaki still fails to disclose each element of the pending claims.

For at least these reasons, Applicants respectfully request that the § 102 rejection of claim 1 and its dependent claims be withdrawn.

Dependent Claims

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Because claim 1 is allowable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also allowable. In addition, it is respectfully submitted that the dependent claims are allowable based on their own merits by adding novel and non-obvious features to the combination.

Based on the foregoing, it is respectfully submitted that all pending claims are patentable over the cited prior art. Accordingly, it is respectfully requested that the rejection under §§ 102, 103 be withdrawn.

Conclusion

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication for which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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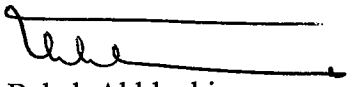

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